PATENTS
174/079Re

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

REISSUE APPLICATION

Application for
Reissue of Patent No.: 5,970,255

Issued : October 19, 1999

Patentee/
Reissue Applicants : Nghia Tran, Ying Xuan Li, Janusz Balicki, and John Costello

For : SYSTEM FOR COUPLING PROGRAMMABLE LOGIC DEVICE TO EXTERNAL CIRCUITRY WHICH SELECTS A LOGIC STANDARD AND USES BUFFERS TO MODIFY OUTPUT AND INPUT SIGNALS ACCORDINGLY

Assignee : Altera Corporation

Box REISSUE
Hon. Commissioner for Patents
Washington, D.C. 20231

October 19, 2001
New York, NY 10020

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97, applicants wish to call the attention of the Examiner to the following references:

U.S. patents
Re 34,808 Hsieh
4,032,800 Druscher et al.
4,472,647 allgood et al.
4,527,079 Thompson
4,625,129 Ueno
4,783,607 Hsieh

	4,791,312 Weick
	4,797,583 Ueno et al
	4,820,937 Hsieh
	4,879,481 Pathak et al.
	4,933,577 Wong et al
	4,970,410 Matsushita et al.
	4,975,602 Nhu
	4,987,319 Kawana
	4,994,691 Naghshineh
	4,999,529 Morgan, Jr. et al.
	5,023,488 Gunning
	5,028,821 Kaplinsky
	5,034,634 Yamamoto
	5,132,573 Tsuru et al.
	5,151,619 Austin et al.
	5,235,219 Cooperman et al.
	5,282,271 Hsieh et al.
	5,300,835 Assar et al.
	5,311,080 Britton et al.
	5,317,210 Patel
	5,332,935 Shyu
	5,374,858 Elmer
	5,428,305 Wong et al.
	5,428,800 Hsieh et al.
	5,534,794 Moreland
	5,534,798 Phillips et al.
	5,589,783 McClure
	5,612,637 Shay et al.
EPO Applications	0 358 501
	0 426 283 B1
	0 544 461 A2
	0 608 515 A1
	0 616 431 A1
Japan Applications	01-274512
	02-013124
	02-161820
	04-223617

B.A. Chappell, et al., "Fast CMOS ECL Receivers with 100mV Worst-Case Sensitivity" IEEE Journal of Solid-State Circuits, Vol. 23, No. 1, February 1988, pp. 59-66.

F. Claude, "Cross-boundry PLDs", Semiconductor Currents, June 1991, pp. 9-10.

Carlo Guardiani, et al., "Applying a submicron mismatch model to practical IC design" IEEE 1994 Custom Integrated Circuits Conference, 1994, pp. 297-300.

Bill Gunning, et al., "A CMOS Low-Voltage-Swing Transmission-Line Transceiver" IEEE International Solid-State Circuits Conference, 1992, pp. 58-59.

Andrew Haines, "Field-programmable gate array with non-volatile configuration", Microprocessors and Microsystems, Vol. 13, No. 5, June 1989, pp. 305-312

H.I. Hanafi, et al., "Design and Characterization of CMOS Off-Chip Driver/Receiver with Reduced Power-Supply Disturbance" , IEEE Journal of Solid-State Circuits, Vol. 27, No. 5, May 1992, pp. 783-785.

"IEEE 1194.1 BTL-Enabling Technology for High Speed Bus Applications", June 1992, pp. 1-5.

K. Knack, "Debunking High-Speed PCB Design Myths", ASIC & EDA, July 1993, pp. 12-26.

M.J.M. Pelgrom, et al., "A 3/5 V Compatible I/O Buffer", IEEE Journal of Solid-State Circuits, Vol. 30, No.7, July 1995, pp. 823-825.

M.J.M. Pelgrom, et al., "Matching Properties of MOS Transistor", IEEE Journal of Solid-State Circuits, Vol. 24, No.5, October 1989, pp. 1433-1440.

B. Prince, et al., "ICS going on a 3-V diet", IEEE Spectrum, May 1992, pp. 23-25.

A.L. Roberts, "Session XIX: High Density SRAMs", IEEE International Solid-State Circuits Conference, February 1987, pp. 252-254.

R. Senthinathan, "Application Specific CMOs Output Driver Circuit Design Techniques to Reduce Simultaneous Switching Noise", IEEE Journal of Solid-State Circuits Conference, Vol. 28, No. 12, December 1993, pp. 1383-1388.

R. Senthinathan, "Simultaneious Switching Ground Noise Calculation for Packaged CMOs Devices, IEEE Journal of Solid-State Circuits Conference, Vol. 26, No. 11, November 1991, pp. 1724-1728.

M. Ueda, "A 3.3V ASIC for Mixed Voltage Applications with Shut Down Mode", IEEE Custom Integrated Circuits Conference, 1993, pp. 25.5.1 - 25.5.4.

S. H. Voldman, "ESD Protections in a Mixed Voltage Interface and Multi-Rail Disconnected Power Grid Environment in 0.50 and 0.25 Channel Length CMOS Technologies", EOS/ESD Symposium, pp. 3.4.1 - 3.4.10, 1994.

T.T. Vu., "A Gallium Arsenide SDFL Gate Array with On-chip RAM", IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 1, February 1984, pp. 10-22.

J. Williams, "Mixing 3-V and 5-V Ics", IEEE Spectrum, March 1993, pp.40-42.

These references are also listed on the attached Form PTO-1449, and copies of them are enclosed.

Consideration of the foregoing in relation to this patent application is respectfully requested.

Respectfully submitted,

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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 174/079Re	APPLICATION NO.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANT Nghia Tran, et al.	
	FILING DATE October 19, 2001	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	Re. 34,808	12/20/94	Hsieh	326	71	
	4,032,800	06/28/77	Dröscher et al.	307	296	
	4,472,647	09/18/84	Allgood et al.	307	475	
	4,527,079	07/02/85	Thompson	307	475	
	4,625,129	11/25/86	Ueno	307	446	
	4,783,607	11/08/88	Hsieh	307	475	
	4,791,312	12/13/88	Weick	307	264	
	4,797,583	01/10/89	Ueno et al.	307	475	
	4,820,937	04/11/89	Hsieh	307	475	
	4,879,481	11/07/89	Pathak et al.	307	465	
	4,933,577	06/12/90	Aso	307	465	
	4,970,410	11/13/90	Matsushita et al.	307	303	
	4,975,602	12/04/90	Nhu	307	475	
	4,987,319	01/22/91	Kawana	307	465	
	4,994,691	02/19/91	Naghshineh	307	475	
	4,999,529	03/12/91	Morgan, Jr. et al.	307	475	
	5,023,488	06/11/91	Gunning	307	475	
	5,028,821	07/02/91	Kaplinsky	307	465	
	5,034,634	07/23/91	Yamamoto	307	465	
	5,132,573	07/21/92	Tsuru et al.	307	475	
	5,151,619	09/29/92	Austin et al.	307	475	
	5,235,219	08/10/93	Cooperman et al.	307	443	
	5,282,271	01/25/94	Hsieh et al.	395	275	
	5,300,835	04/05/94	Assar et al.	307	475	
	5,311,080	05/10/94	Britton et al.	307	465	
	5,317,210	05/31/94	Patel	307	465	

EXAMINER DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.

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	5,332,935	07/26/94	Shyu	307	475	
	5,374,858	12/20/94	Elmer	327	333	
	5,428,305	06/27/95	Wong et al.	326	75	
	5,428,800	07/27/95	Hsieh et al.	395	775	
	5,534,794	07/09/96	Moreland	326	63	
	5,534,798	07/09/1996	Phillips et al.	326	108	
	5,589,783	12/31/96	McClure	326	71	
	5,612,637	03/18/97	Shay et al.	326	86	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	01-274512	11/02/89	Japan				
	02-013124	01/17/90	Japan				
	02-161820	06/21/90	Japan				
	04-223617	08/13/92	Japan				
	0 358 501	09/07/89	EPO				
	0 426 283 B1	05/08/91	EPO				
	0 544 461 A2	06/02/93	EPO				
	0 608 515 A1	08/03/94	EPO				
	0 616 431 B1	09/21/94	EPO				

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